Demonstration of Low Power Stream Processing Using a Variable Pipelined CGRA
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Introduction
CGRAs (Coarse-Grained Reconfigurable Architectures) are expected to be used for IoT devices and edge computing due to their high energy efficiency. VPCMA (Variable Pipelined Cool Mega Array) is a low power CGRA which we previously proposed in [1]. CC-SOTB2 is a real chip implementation of the VPCMA using Renesas 65-nm SOTB technology [2]. In this demonstration, we will show the low power consumption of the CC-SOTB2 while performing a real image processing with a tiny solar cell battery.

Architecture Overview

VPCMA (Variable Pipelined Cool Mega Array)[1]

- PE (Processing Element)
  - Composed of
    1. Simple ALU
    2. Switching Element
    3. No Register file
    4. No need of clock signal
- PE Array
  - 12 cols x 8 rows PEs
  - 7 configurable pipeline regs. (Latch mode/Bypass mode)
- Variable Pipeline
  - Trade-off b/w performance & power consumption
- Micro-controller
  - Controls data transfer b/w data memory & PE array
- External host processor
  - Uses common data bus for data transfer, reconfiguration, and other controls

A Real Chip Implementation: CC-SOTB2

- A prototype chip of VPCMA: CC-SOTB2
  - Fabricated with Renesas SOTB technology
  - 3mm x 6mm die
- About SOTB technology
  - 65 nm process
  - Good for body bias control
  - Trade-off b/w power & transistor performance
- Five body bias domains in CC-SOTB2
  - PE array’s domains vs. micro-controller’s domain
    - Adjust the balance of performance b/w PE array & micro-controller
  - Four divided PE array’s domains
    - Boost only bottleneck PEs & slow down other PEs

System Overview

Programming and Computing with a Host CPU

- Application Development Flow
  - Program (C Code)
  - C Compiler (clang)
  - LLVM IR
  - Extract Loop Kernels
    - Data Flow
    - Loop Kernels
    - GA-based Mapping Optimizer
    - Mapping Optimization[2]
      - Mapping Data-Flow-Graph in the loop to PE Array
      - Genetic-Algorithm-based Optimization tool
    - Full automated flow is under development
- Computation with Zynq FPGA
  - Zynq-PL (FPGA)
  - Zynq-PS
    - Linux OS
    - API for the Linux OS

Demonstration Environment

- Motherboard for experiment & demo
  - Connects CC-SOTB2 with Zynq FPGA
  - Power supply boards are available
    - Voltage control by Zynq
  - In this demonstration, a tiny solar cell battery
    - Large internal resistance
    - Voltage is kept only for extremely low power systems

Results of Image Processing

- In the best case (sf),
  - About 3 mW peak power
  - 80 PEs utilized
    - 2.4 GOPS / 3 mW
  - Up to 30MHz, the real chip can work stably with 0.55 V
- Gray Scaling of RGB image

Reference: